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PAGE 1/3 * RCVD AT 8/5/2005 6:34:55 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-6/25 * DNIS:2738300 * CSID:Haynes and Boone,LLP * DURATION (mm:ss):00:48

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:
Chi-Chun Chen, et al.

Serial No.: 10/600,393

Filed: June 20, 2003

For: METHOD OF FORMING DUAL
GATE INSULATOR LAYERS FOR
CMOS APPLICATIONS

Attorney Docket No.:
002-0066 / 24061.461

Customer No. 42717

Group Art Unit: 2822

Examiner: Tomise M. Thomas

Confirmation No.: 8529

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Kelly A. Moreau

Sir:

COMMENT ON STATEMENT OF REASONS FOR ALLOWANCE

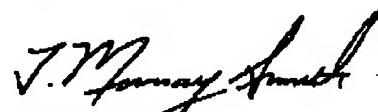
Applicants acknowledge receipt of the Notice of Allowance mailed on July 12, 2005, which was accompanied by a Notice of Allowability (Form PTOL-37). Page 2 of the Notice of Allowability sets forth a statement by the Examiner of reasons for allowing certain claims. Applicants agree that the claims recite allowable subject matter. However, Applicants do not agree in all respects with the stated reasons for allowance. For example, Applicants respectfully submit that the stated reasons should not be interpreted to mean that there are no other reasons

Appl. No. 10/600,393
Comment on Statement of Reasons for Allowance

Attorney Docket No. 2002-0066 / 24061.461
Customer No. 42717

which separately and independently support the allowability of the independent claims and/or the dependent claims.

Respectfully submitted,



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Date: August 5, 2005

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Enclosures: None

R-112806.1